Atacama Large Millimiter Array
2nd generation MMIC sampler for ALMA
Design report

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Abstract

A sampler circuit for the Atacama Large Millimeter Array, based on a GaAs 0.12 mm process, has been designed and tested by simulation. The use of a separate sampler before the BiCMOS digitizer allows a longer time for quantization decision, and reduces the timing requirements on the digitizer. The predicted performances fulfills the requirements for the ALMA sampler/digitizer. In particular the aperture time is < 50 ps, and the bandwidth in excess of 4 GHz. A first version of the chip has been fabricated, but a layout error prevents it from operating correctly. Recovery actions are being attempted, but it is difficult that a working unit will be available in due time.

1-INTRODUCTION.

Atacama Large Millimeter Array (ALMA) [9] is composed by 64 to 80 radio telescopes of 12 m diameter, operating from 31 to 950 GHz. It will be sited in the Atacama Altiplano in northern Chile, at an altitude of 5000 m, north of the VLT site, and is planned to become operative starting from 2005, with full capability in 2010. Each antenna observes a maximum bandwidth of 8 GHz, implemented as four 2 GHz sub-bands, simultaneously in two polarizations. Thus, a total of 8 independent radio signals (IF's), with a bandwidth of 2 GHz each, is generated by each antenna.

The output of each IF is represented by a signal at nominally 0 dBm (0.23V RMS), with a bandwidth comprised between 2 and 4 GHz. It must be sampled and quantized to a stream of 3-bit digital samples (8 levels), at a rate of 4 MS/s.

Quantization is operated by a sampler/digitizer unit based on Track & Hold (T&H) circuit designed by Arcetri Observatory and the Microelectronic Laboratory of University of Florence, and a SiGe digitizer the Electronics Engineering department of the University of Bordeaux[11].

The introduction of a Track and Hold (T&H) in the quantization chain, commonly used in multi-bit flash digitizers, is useful to overcome non ideal behavior of the comparators, especially in their dynamic performances (e.g. skew in propagation delay, or its dependency on signal amplitude). This technique consists in first sampling the signal, using a T&H circuit, and then digitizing the stable samples so obtained.

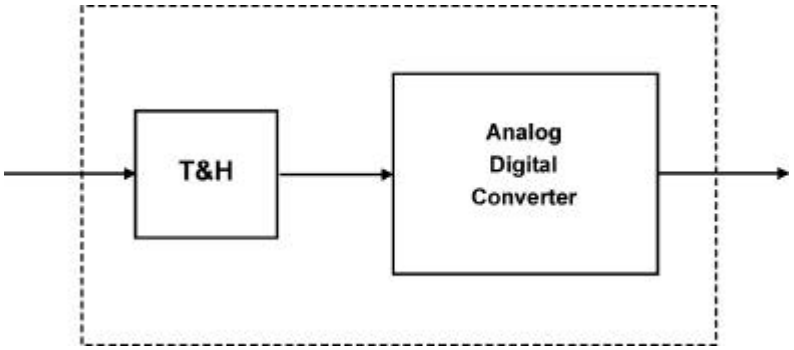

Fig. 1: Sampler/digitizer unit

It should be noted that the digitizer can operate without a T&H. This unit has thus been designed in such a way that it should be possible to remove it from the digitizer unit without redesigning other components. The main requirement for this is that the unit must have the same input and output specifications

A first prototypes of a Track and Hold circuit (T&H) for ALMA has been designed in Arcetri in late 2001. This unit has shown minor design problems, in particular the need for several supply voltages and input/output mismatch. With the experience of this first design, a second generation T&H has been designed and fabricated.

Tab.1 ALMA track & Hold Requirements

Requirements	
INPUT SIGNAL BANDWIDTH:	2 GHz (2 - 4 GHz)
Sampling Frequency :	4 GHz
Bandwidth Ripple:	0.5 dB
Clock Signal:	0.5 Vpp (Nominally Sinusoidal)
Square Wave Clock	internally generated
Square Wave Rise Time and Fall Time	50 ps
Internal clock jitter	<5ps
Square Wave Clock Duty Cycle:	50%
Nominal Input signal level	0 dBm (230 mV RMS) Gaussian noise
Acceptable Input Signal Level	+/- 10 V, clipped at +/- 1.6V
Accuracy	2.00%
System Impedance:	50 Ohm

1.1 Module Interface

The T&H module receives a RF signal, at nominal 0dBm, from the IF processor, and delivers a sampled RF signal to the digitizer, at about 0 dBm. It has been shown difficult to have exactly 0 dBm insertion loss, and thus either the signal from the IF processor should be increased by ~2dB, or the digitizer should be able to digitize a signal at -2dBm. No other modifications are needed when inserting or deleting this unit between the IF processor and the digitizer.

The module requires a 4 GHz clock, sinusoidal, 0dBm nominal, correctly phased with respect to the digitizer clock. The relative phase of the two clocks is fixed, TBD. The T&H produces a stable output in an interval of 60-160 ps with respect to the rising edge of the clock sinewave.

The module requires two supply voltages, at +/- 2.5V, 160 mA.

No control or monitor connections are required.

The module is physically delivered as a naked chip, 1x1.5 mm in size, to be bonded in a multichip module. A connectorized version has been built, but is too expensive and bulky for production volumes.

2 - CIRCUIT DESCRIPTION

2.1 - Introduction

The 2nd generation T&H has been conceived as an evolution and a refinement of the first generation one, described in [Arcetri Technical Report n. 2/2001] .

The circuit is based on a self inverting FET switch configuration which is compatible with the requirements of large input signal dynamic and high sampling rate.

One of main characteristics of this configuration consist of the use an unbalanced square wave clock signal to drive the switch. This greatly simplifies clock generation starting from a single ended sinewave, with respect of a diode bridge switch solution that requires complementary clocks. Another important feature of this topology is the small die area required.

As stated in the [Arcetri Technical Report n. 2/2001] the most important errors affecting the sampling circuit are related with the non ideal behavior of the FET switch. These error are:

1. *Aperture time:* It is due both to finite rise time in the generated clock signal, and finite response time in the switch. Produces attenuation at the higher input frequencies and non ideal frequency response
2. *Feedthrough:* It is due to cross-talk between the switch input and output due to parasitic capacitance in the hold state
3. *Jitter error:* non deterministic phase error in the clock signal. It seriously degrades the phase response of the sample

The optimum performances of self inverting FET switch in terms of *feed through* and *accuracy* have been confirmed by the measurements made on the prototypes of the switch belonging to the first run. These results lead to confirm the choice of the switch configuration for the 2nd generation T&H.

The new circuit has been implemented using the same architecture developed for the first one. The functional blocks of the circuit are reported in Fig.2 and are the same of the 1st generation.

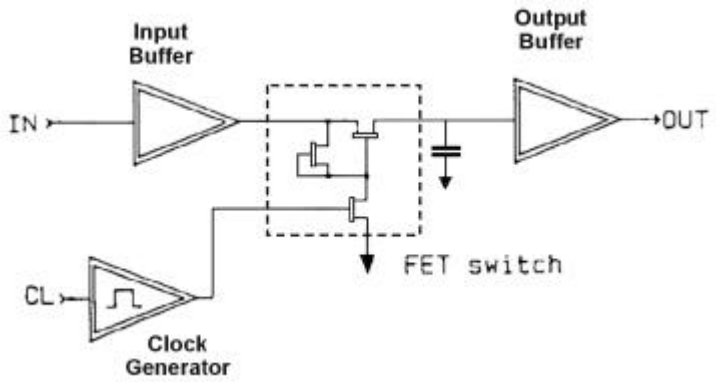

Fig. 2: Architecture of the Track & Hold circuit.

The blocks themselves have been redesigned, to overcome the problems encountered i the first version. Most of these problems iwere related with an incorrect evaluation of the maximum dynamic of the input signal. As a consequence the 1st generation circuit was designed on the base of a input signal level around 10 dBm, instead of the 0 dBm reported in Tab.1. In the new design, the buffers have been redesigned in order to improve the output impedance and to require only two supply voltages. The clock generator now operates with the same supplies, ad requires considerably less power. The 2nd generation T&H makes also use of a slightly modified self inverting FET switch with respect of the one implemented in the first version.

The new T&H has been developed following the system on a chip approach. All the functional blocks (Fig.2) have been implemented on the same chip, including the level shifting circuits for the generation of the biasing dc levels, and all the choke capacitance need to ensure the absence of spurious signal on bias voltage. Only external voltages of +2.5V, -2.5V.

As the previous version, this chip has been implemented using the OMMIC ED02AH P-HEMT process. This technology is available for prototyping and small volume production through Circuits Multi Project (Grenoble).

The main features of ED02AH technology are summarized below [3]:

1. Hetero-epitaxy with a pseudomorphic (GaInAs) active layer
2. Depletion and enhancement mode recessed transistors: Vt=0.1V or -0.9V
3. 2 types of diodes (0.2µm "GM" and 3µm "BE") for mixing, level shifting, or varactors.
4. Resistors, using the GaAs active layer, non etched.
5. Full Si_3N_4 protection ensuring high reliability
6. 2 types of MIM capacitors, using the Si_3N_4 layer and the Si_3N_4 + SiO_2 layer.
7. SiO_2/Si_3N_4 + air bridge isolation between layers to reduce the parasitic capacitances.
8. High yield 1.25µm thick gold metallization for interconnections and spiral inductors. Possibility of multi metal lines to reduce series resistances.
9. Via holes through the 100µm substrate to reduce parasitic inductances to ground.

2.2- Schematic Block Diagram

The sampler is organized on the base of a certain number of functional blocks, shown in Fig. 3.

1. *Clamping circuit:* (based on diodes) guarantees the protection against high level input signals, effectively shorting to ground signals greater than about 1.8V.
2. *Input buffer*: ensures high input impedance and provides the low impedance required to drive the sampler switch.

3.*Switch and the hold capacitance*: implements the sampling function,

4.*Clock generator*: provide the square wave clock signal.

5.*Output buffer*: supplies the high input impedance that must be seen by the hold capacitance, and the required 50 ohm output impedance.

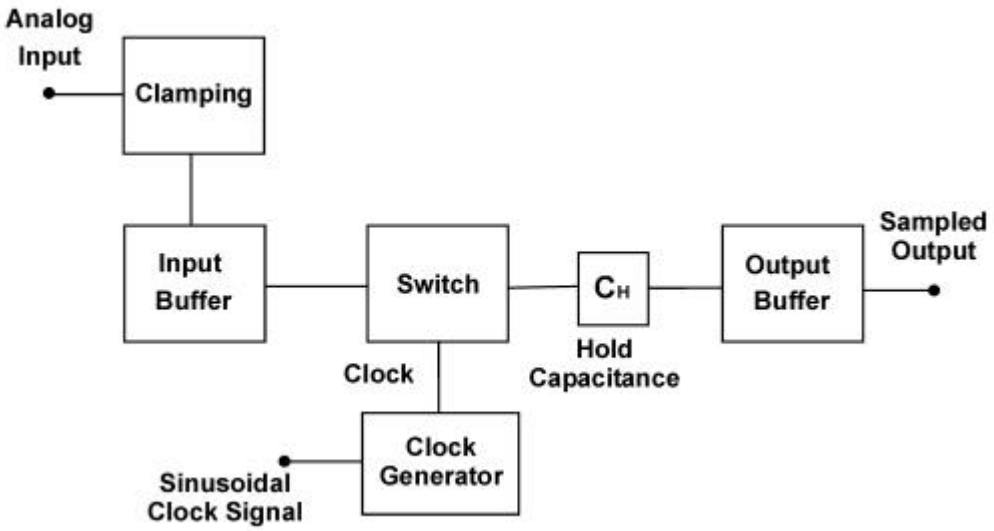

Fig. 3: Track & Hold circuit block diagram.

The clamping circuit begins to affect the signal at about 1.2V, and shows absolutely no effect for signal amplitude below 0.8V, corresponding to more than tree times the expected RMS value. As the last threshold in the digitizer is at about 1.8 times the RMS value, the voltage interval affected by the clamping is always mapped in the more extreme digital codes. Clamping the input voltage results also in a faster recovery from high signal spikes.

2.3 - Sampling Circuit

As stated above, the T&H circuit has been implemented using a FET Self Inverting Switch architecture, a configuration based on a shunt series topology. Its schematic is shown in Fig. 4.

One of the most important feature of this topology is the self inversion of the clock signal supplied by the shunt branch, that enable the use a single clock signal to drive both shunt and series switch. This approach allows a great simplification in the clock generation circuit, avoiding the problem related with a balanced square wave required in the diode bridge and differential FET switch. [4], [5],[6]

A few modifications have been introduced with respect of the first version as a consequence of the decrease in the required dynamic of the input signal. The negative supply voltage is -2V instead of -4V, and the switch FET ratio has been modified. Also

the hold capacitance has been modified in order to optimize the performance of the sampling block. In particular the new version of the circuit shows better performance both in the track interval of the sampling period and in the hold interval.

The simulated performances of the Sampler Circuit are shown in Fig.5. The small signal S transmission parameter (S21) in the track (blue) and hold (red) interval of the sampling period shown the good performance of the implemented circuit. Wit an insertion loss of 1.60 dB in the whole bandwidth and an isolation of at least 30 dB at 4GHz.

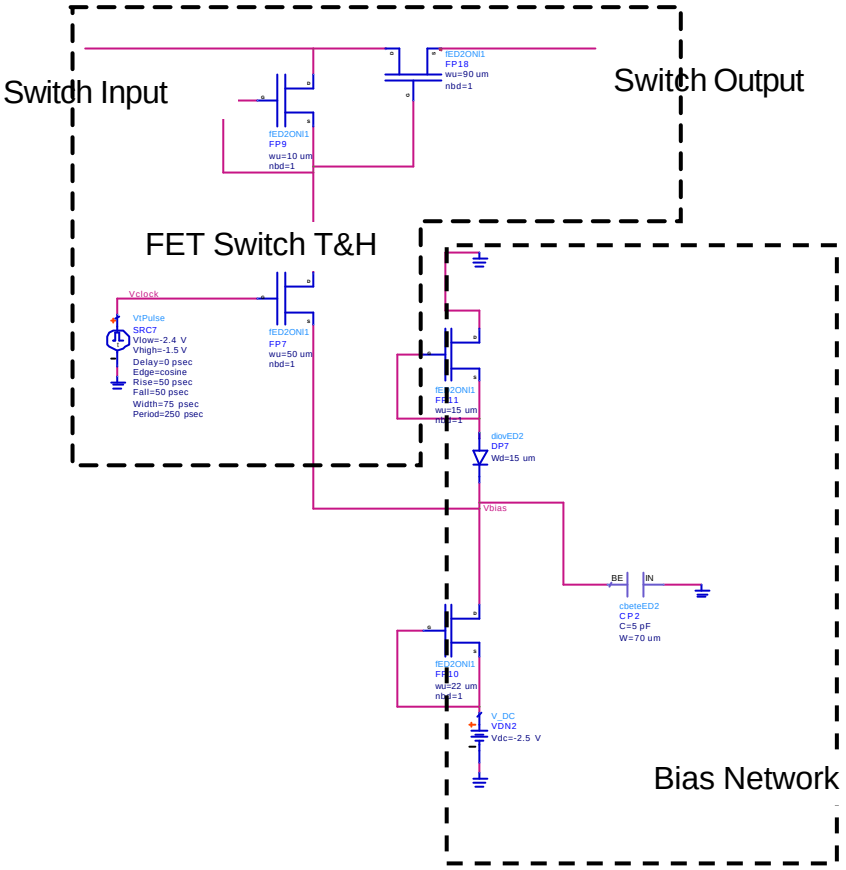

Fig. 4 - Sampler Circuit

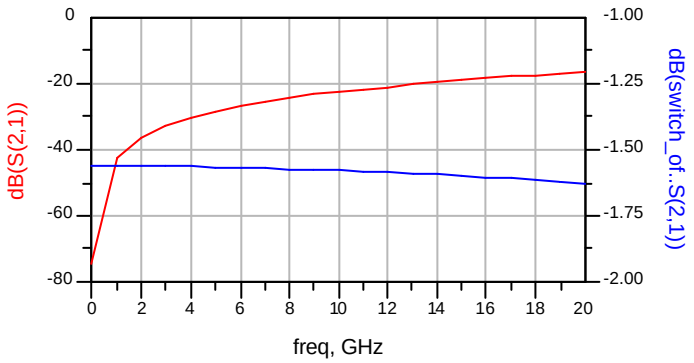

Fig. 5 - Small Signal performance of the Sampler Circuit

2.4 - Clock Generator

This block generates the square wave clock signal from the 0.5 Vpp clock sinusoidal signal supplied from the system. Its schematic is shown in Fig. 6.

From a general point of view the circuit is composed by a common source stage followed by a common drain. [7]. The first stage generates the quasi square wave signal while the other behaves as a buffer offering the first stage an high input impedance. The buffer stage provides a signal with the low output impedance needed to drive the gate of the sample the sample and hold circuit. The DC supply voltage of the common source is derived from the -2.5V supplied to the chip. The circuit is AC coupled to the clock sinusoidal input signal while the output is dc coupled to the electronic FET Switch.

In Fig. 7 the square wave generated by the circuit is shown, superimposed to the corresponding ideal square wave. The comparisons between the ideal and real clock signal highlight a good agreement with the specification and in particular a rise time of about 50 ps that is mandatory for the optimum behavior of the circuit.

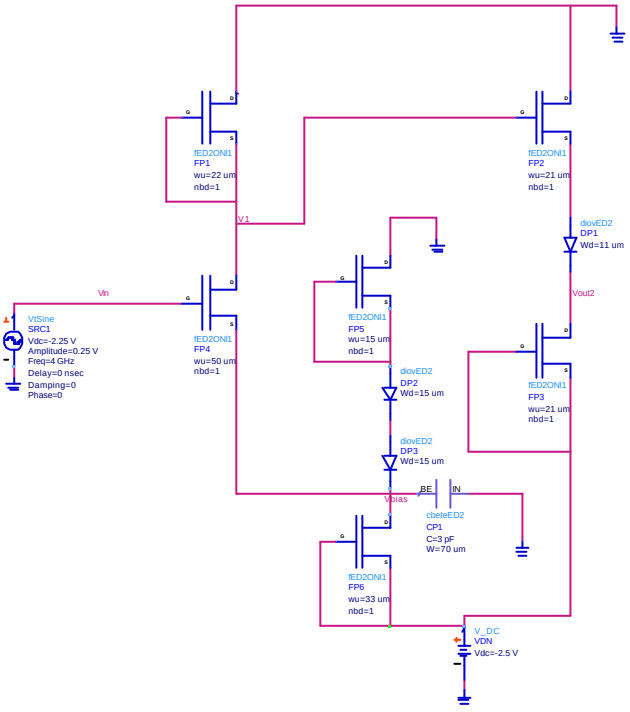

Fig. 6 - Schematic of Clock Generator circuit

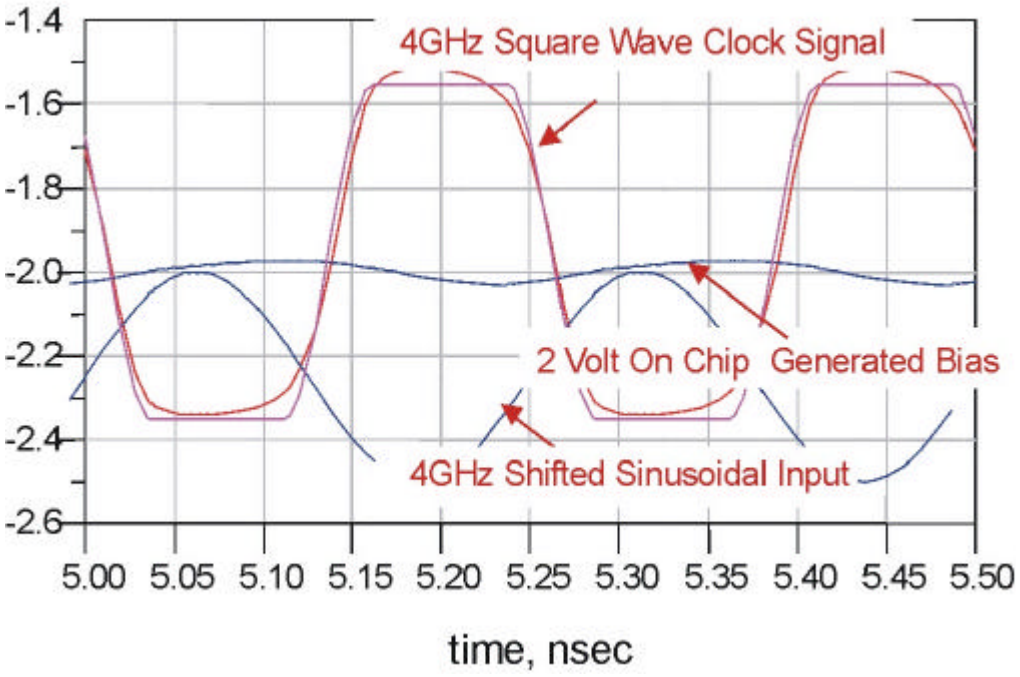

Fig. 7 - Square wave generated by clock generator

2.5 - Input and Output Buffers

One of the main modification introduced in the second version of the circuits consist of a completely new topology for the input and output buffer. The new configuration have been chosen due to a better response in terms of input impedance and power consumption. A high input impedance is needed in the output buffer in order to prevent a quick discharge of the hold capacitance in the hold phase.

The supply voltages have been modified with respect of the first version (+/- 2.5V instead of +/- 3V). This produces a reduction in the DC power but requires a more complex circuit topology. The introduction of a current mirror in the output stage improves the output driving capability for a low value of the output impedance. This feature is very important characteristic for the input buffer that has to drive the lo imput impedance shown by the input of the FET switch.

This buffer, which schematic is shown in Fig. 8, is a complex version of the source follower configuration, optimized to maximize the input and minimize the output impedances. The circuit is also designed to minimize the insertion loss and maximize the bandwidth. This aspect is very important for the output buffer, that must deals with the high order harmonics generated in the sampling process.

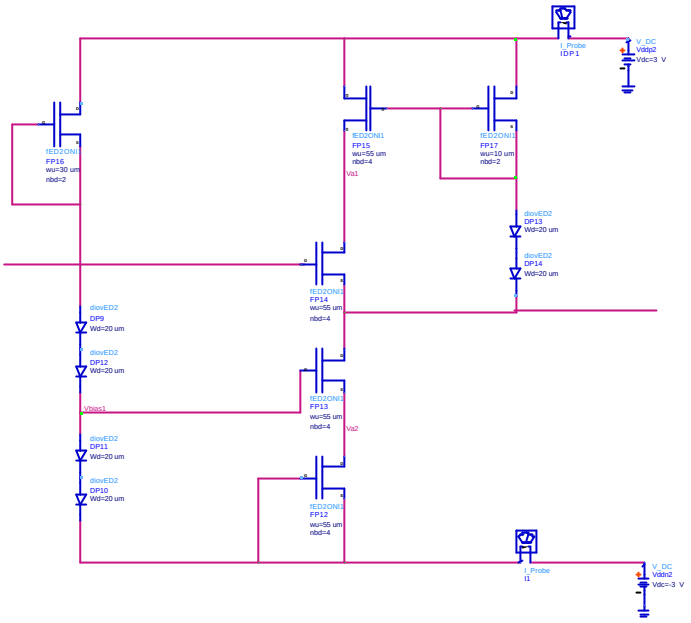

Fig. 10 - Input and output buffer circuit.

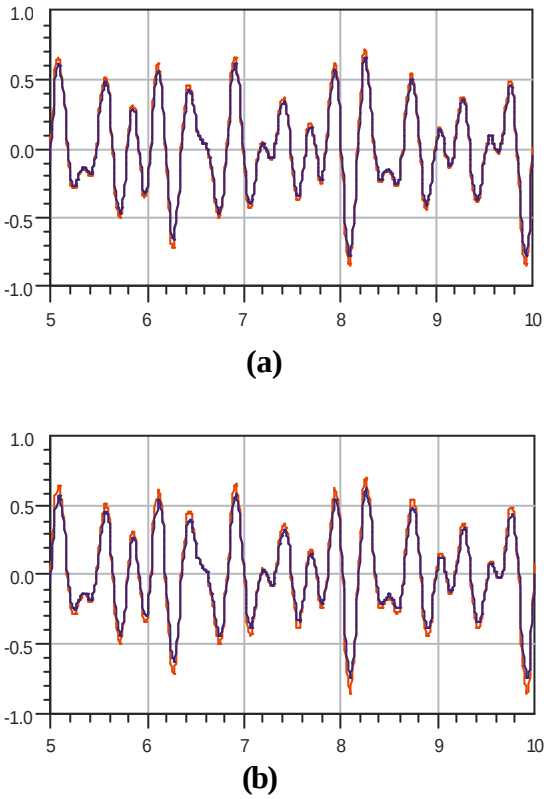

Fig. 9 - Buffer response to a composite signal on different load: 1kΩ (upper) and 50Ω (lower)

Fig. 9 shows the good performance of the new buffer configuration in driving a low impedance (50 Ohm) load. This is necessary because the T&H is physically separated

from the digitizer, and thus requires a matched transmission line. A modest attenuation (10%, ~1dB) is present due to the finite output impedance.

2.6 -Layout

Circuit layout is shown in fig. 10, with functional blocks highlighted. Chip dimensions are 1.5x1 mm. Input, clock and output pads are configured for 3-finger radiofrequency probes, with finger spacing from 150 to 200 ?m. The production chip will have only bonding pads, thus reducing chip size.

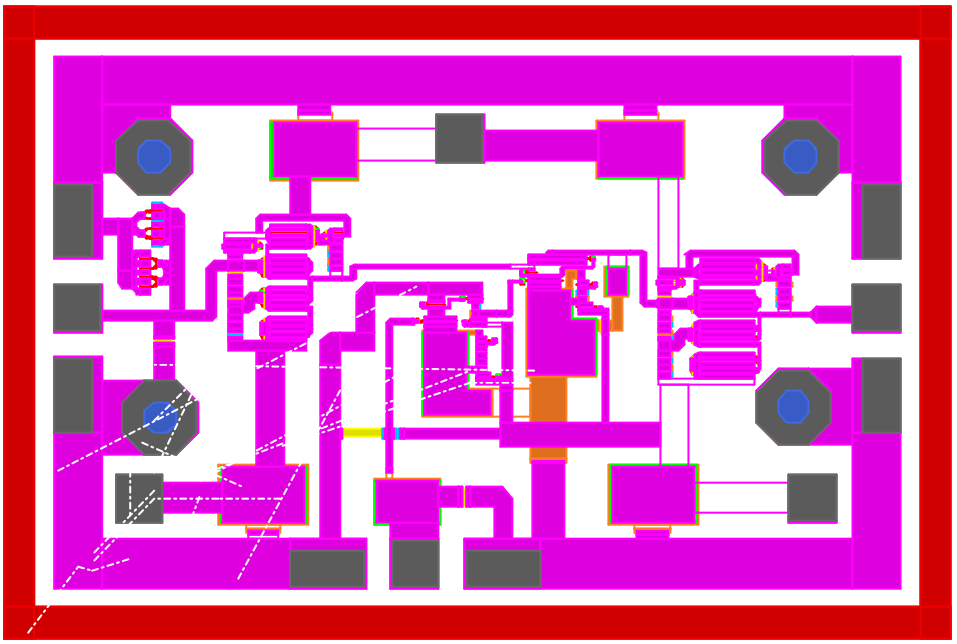

Fig 10 - Circuits Layout of the Track and Hold

3 - SIMULATED TESTS ON THE CIRCUIT

3.1 - Introduction

The circuit performances has been evaluated simulating a series of tests. All tests have been performed using the Agilent ADS2002 Microwave CAD Simulator and the device models provided by the manufacturer (ED02AH library version 2.5 from OMMIC through CMP) [8] for this process. ED02AH 2.5 library has shown in previous experience a very good performances in predicting the actual behavior of circuits manufactured using this technology.

3.2 - Simulation Results

A certain number of different simulation have been implemented in order to evaluate the performances of the T&H. In the following the results of the simulation will be shown. Many of this virtual experiment has been developed in order to compare the predicted performances with the measured one.

Fig. 10 show the the performances of the circuit with a composite input signal in the 2 - 4GHz bandwidth. The circuit shows good characteristics in both the track and hold phase of the circuit.

Being the amplitude of the input signal less than the clamping voltage (1.2V) it is clear the absence of spurious effects of the ant parallel couple of diodes at the input of the circuit.

The output signal doesn't show, in the hold phase discharge effect. This means good performances of both the switch FET and output buffer. In particular the output buffer offer an high input impedance to prevent the hold capacitance discharge.

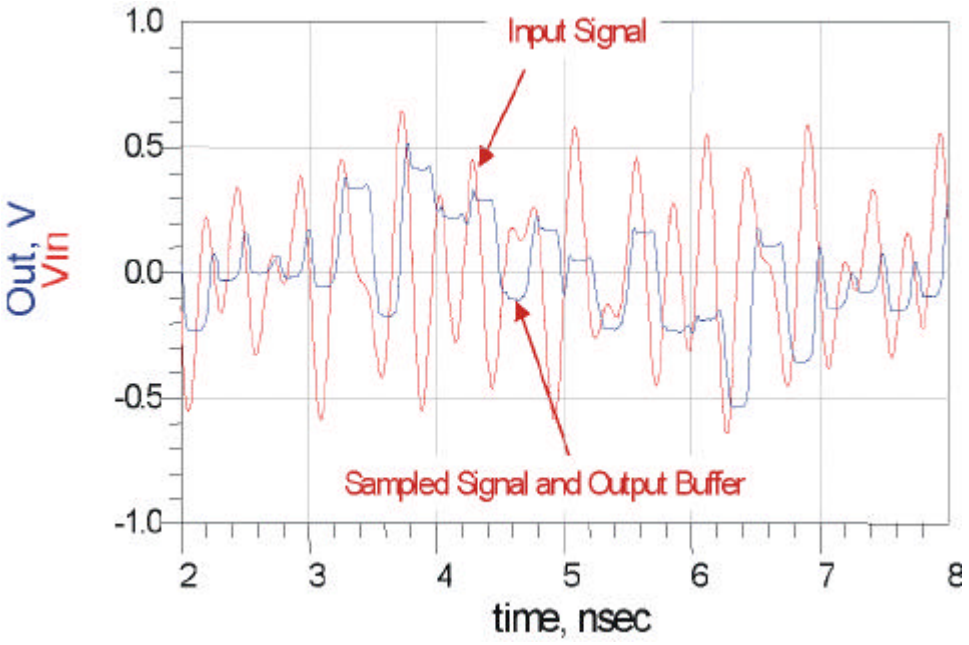

Fig.13- Sampler performances on a composite input signal in the 2-4 GHz band

The simulated performance of the circuit in the 1 - 6 GHz bandwidth has been evaluated following the approach described in Fig.14. A certain number of simulation have been carried out by means of a single tone input signal of the same magnitude and phase but at different frequencies. For each simulation the output data has been resampled and interpolated, and then compared to the input to evaluate the insertion loss, the variation in the phase and the offset introduced from the T&H circuit. The sampled output is resampled in different moment of the sampling period, to evaluate the stability of the T&H output and the valid output window.

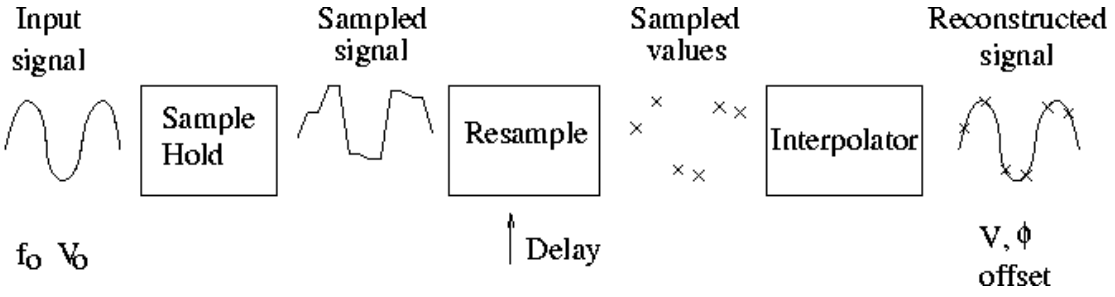

Fig. 14 - Procedure implemented for the evaluation of the performance.

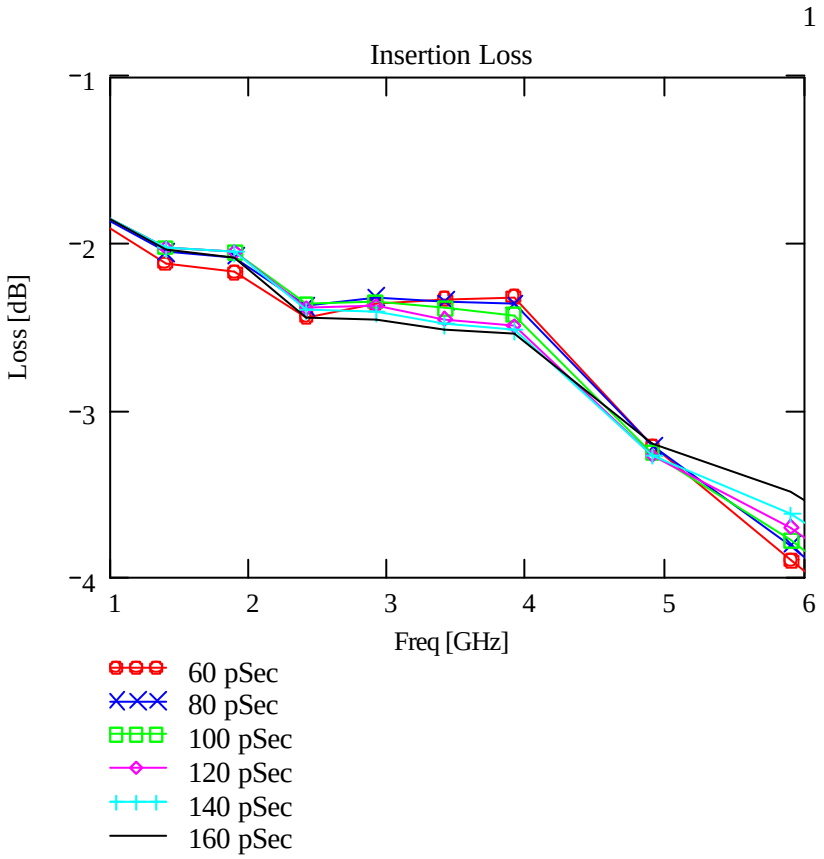

Fig.15 - Simulated insertion loss introduced by the T&H at different sampling instant

Fig.15 shows the evaluated insertion loss introduced by the T&H in the 1- 6 GHz bandwidth. The different curves show the behavior of the circuit across the output window. The output signal is stable in the window 60-160ps with respect to the input clock. The reconstructed signal is 2.3 dB under the input amplitude with less than 0.5 dB of ripple in the 2 - 4 GHz bandwidth.

The Fig.16 shows the DC offset introduced in the 1 - 6 GHz in the reconstructed signal. This offset is always less than 0.04V. Some clock feedthrough causes a DC offset near the clock frequency.

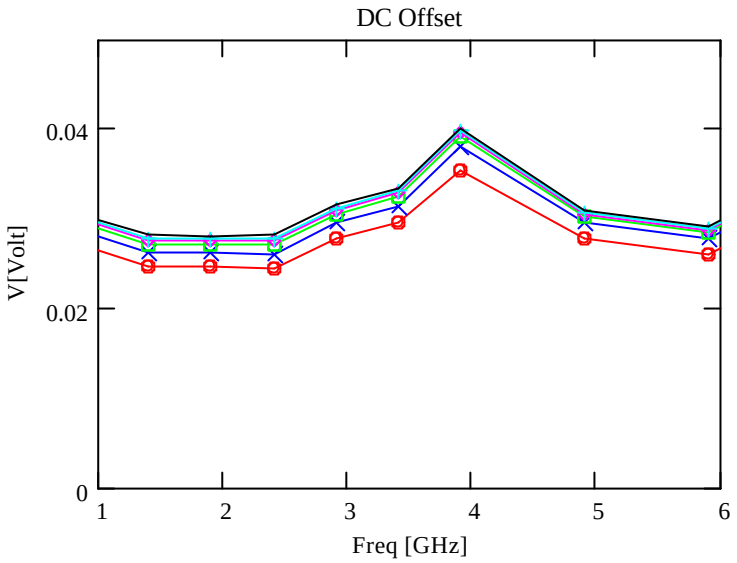

Fig.16 - Simulated DC offset introduced by the T&H. Colors as in fig. 15

Fig. 17 shows the phase offset introduced in the 1-6 GHz interval. For every sampling instant the phase introduced by the circuit is less than 2 deg in the 2 - 4 GHz bandwidth.

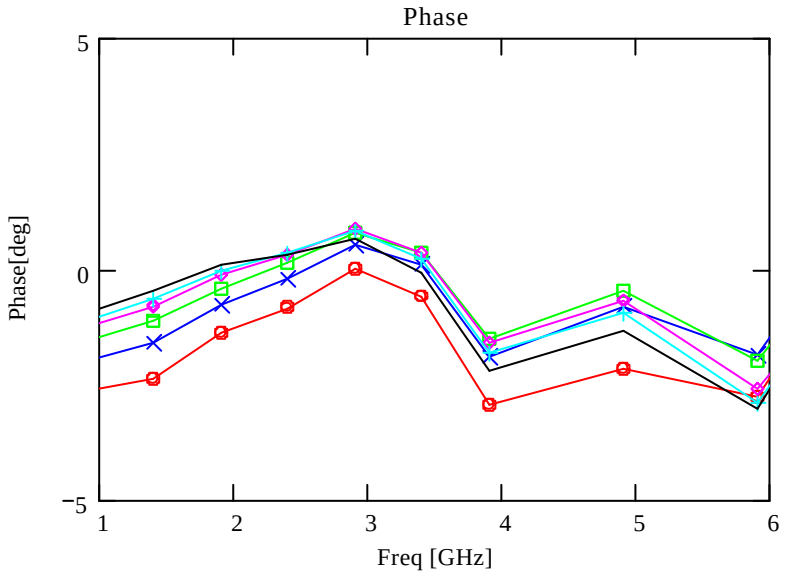

Fig.17 - Simulated phase error introduced by the T&H with respect of different sampling instant

Fig.18 shows the circuit response for one of these simulations, with a input signal of 3.9 GHz and a clock signal of 4 GHz.

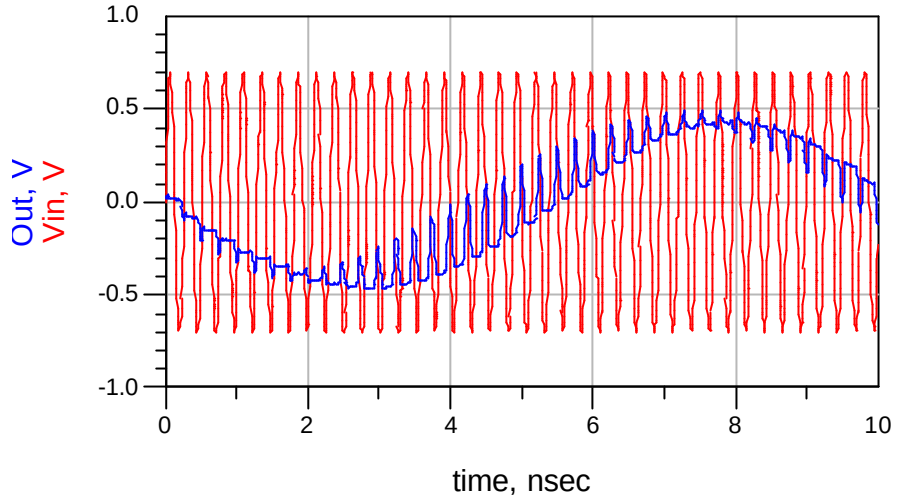

Fig.18 - Time domain response of an input signal @ 3.9GHz and a clock @ 4GHz

In fig. 19 the spectrum of the output signal is shown. This is mostly important to as a base for comparison with the measured spectrum, as the sampled signal spectral content is not particualrly meaningful. The most important harmonic components contained in the output signal are the 100MHz and the ones at the input signal and clock frequencies. In particular the 100MHZ components is the most important component of the spectrum and is the result of the intermodulation product among the input signal and the clock signal.

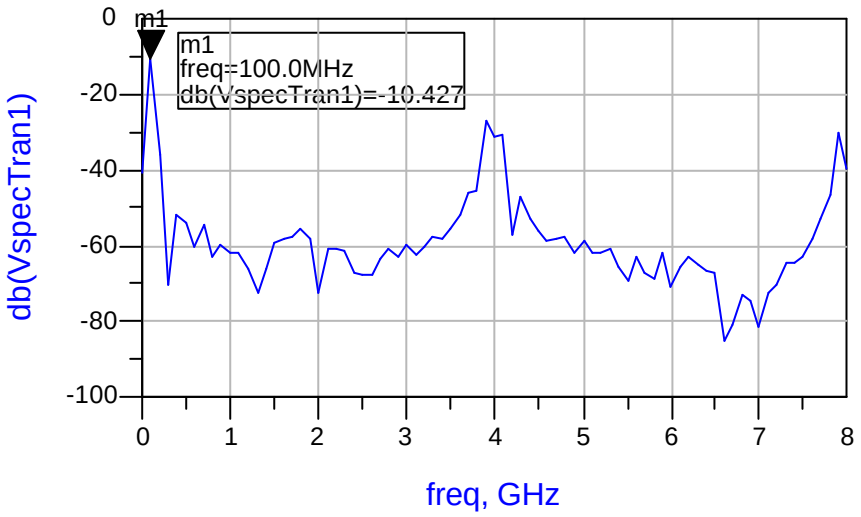

Fig.19 - predicted spectrum of an input signal @ 3.9GHz and clock @ 4GHz

3.3 - Performances

The T&H circuits offer the following performances in term of simulation

1. Aperture time is better than 50 ps. It depends somewhat on the input signal level, being larger for large signals.
2. Insulation in the hold state is 38 dB. Some feedthrough is visible, especially with the large swing Gaussian signals. A compromise between insulation and aperture time has been found optimizing switch FET dimensions and hold capacitance.
3. The hold time is around 100 ps. It is limited by the settling time of the switch after the closure, and by the finite clock transition time at the end of the Hold period.
4. Evaluation of the clock square wave signal generated inside the chip has shown a rise time and fall time of about 50 ps and 52ps.
5. Input VSWR never exceeds 1.25 (S11 < -19 dB) over the whole input band.
6. Insertion loss is 2 dB. This corresponds to a voltage gain of 0.8, and requires that the thresholds of the quantizer must be reduced appropriately. Most of the insertion loss is due to voltage division between the buffer output impedance and the output load. If the digitizer input impedance is increased, the insertion loss is reduced to 0.5 dB (voltage gain of 0.95).
7. The bandwidth has a roll-off of 0.5 dB from 2 to 4 GHz. This is more than the 0.5 dB specification.
8. The frequency response of the output buffer is flat up to 20 GHz

4 TEST AND MEASUREMENTS

4.1 - Introduction

The circuit was sent to the foundry for manufacturing in September 2002, and came back to Arcetri in January 2003. In the meantime, a test protocol was studied and a test jig was built.

The test protocol was developed in order to cover the certification of all the requirements. Protocol include the following measurement.

1. Power supply verification
2. Small signal S-parameter measurement.
3. Low frequencies time domain test (using the instruments available at Osservatorio di Arcetri and Laboratorio di Microelettronica).
4. High frequencies time domain test (using the instruments available at University of Roma - Tor Vergata).

4.2 The Test fixture

A connectorized box (test fixture) was built in order to allow testing on the chip using standard SMA cabling, instead of a a probe station and SGS probe. This box allows also an easier integration to the existing digitizer test fixture, comparing its performance with and without the T&H unit.

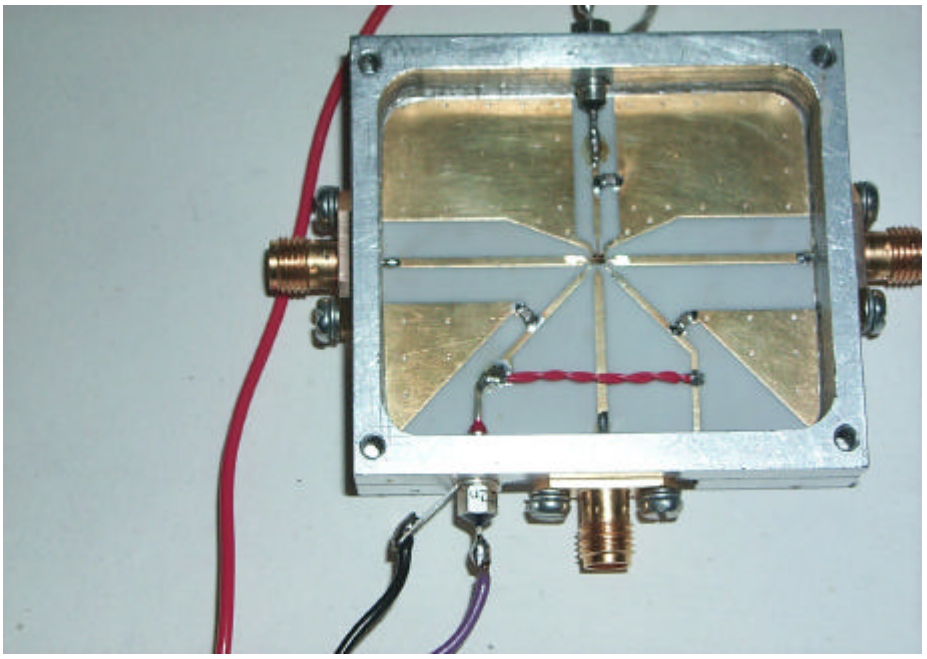

Fig. 20 - T&H test fixture, holding the chip

This unit was built using all the facilities available in Osservatorio di Arcetri with the exception of the microwave printed circuit board. It consists of an aluminium box of 5x6 cm with DC and RF connectors, and a microwave printed circuit board inside. The T&H chip is mounted on the board and connected to the 50Ω microstrip by 25um gold wire bonding. Fig. 20 shows the photo of the complete test-fixture.

The printed circuit board uses high performance plastic substrate, RO4003, 0.508 mm thick and has been designed with the ADS tool. The board was produced by an external supplier with good expertise in this field of application .

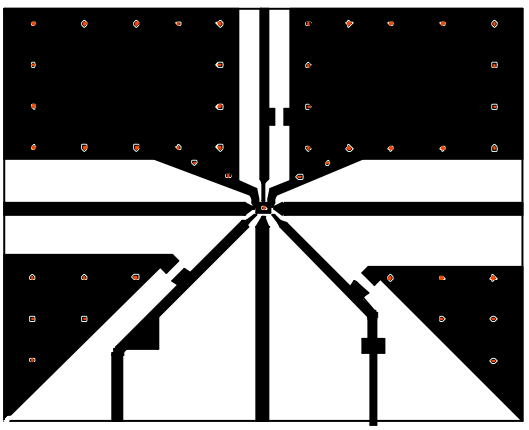

Fig. 21 - RF printed circuit board for T&H test fixture

RO4003 was chosen due to its optimum behaviours in the frequency range of interest. Fig.21 shows the PCB layout. The circuit is gold plated in order to improve the performance of the bonding wire.

Fig. 22 highlights the connection among the printed board and the board and the chip of the T&H. the PCB was designed in order to minimize the wire length to prevent high inductive effect in the input, output and clock signal.

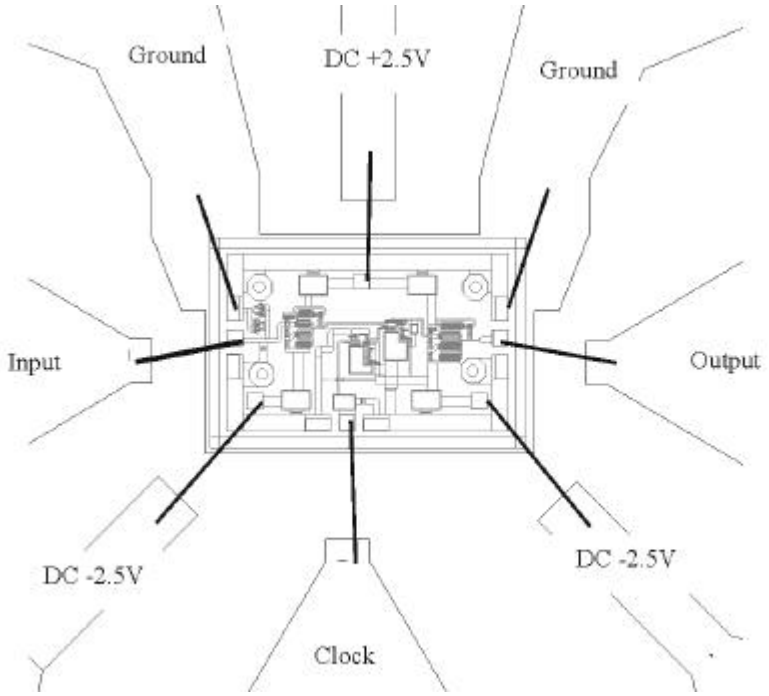

Fig. 22 - Bonding connections from printed circuit board and the T&H chip

4.3Test problems

No measurements have been done until now due to a major problem in the circuit. The problem is related to an error in the layout, that consists in a wrong connection among two FET in the input and output buffers. The error was unnoticed until the first functional tests, and could not be corrected by simple means.

This is not a conceptual error, but doesn't allow the circuit to work correctly. In particular the two wrong connections don't let the correct polarization of the in and out buffers. The drain contact of the buffer remains floating and the functionality of the two buffers is completely compromised. In this situation no measures can be carried out on the chip

4.4 Possible workarounds

The obvious solution for this problem is to resubmit the chip tp the foundry. However, CMP performs only two runs per year, and the next delivery date for this process is in December. We are thus exploring in parallel other possibilities.

- Using the 1st version of the chip. This requres a complete redesign of the test board. The old design requires many supplies, and performs significantly different from this unit to provide useful test data.
- Ion beam litography technique can be used to severe the wrong connections, and to form a new connection.
- A laser used in a microelectronics lab can do a similar work, by cutting the wrong connection and removing the passivation where the new connection must be realized.

We are currently contacting some microelectronic labs to explore the feasibility of these approaches.

5 CONCLUSIONS

The circuit has been designed and simulated, but the fabricated component, due to a clerical error in the layout, does not operate at all. We are currently trying to recover the existing chip, but the result is uncertain. A new chip will be available in December, well beyond every conceivable sampler milestone.

6 BIBLIOGRAPHY

1 "*A 2.5 GHz GaAs sample and hold*" Naber, J.F.; Singh, H.P.; Sadler, R.A., IEEE International Symposium on Circuits and Systems, 1990 Page(s): 3077 -3080 vol.4

2 "*1 GHz GaAs ADC building blocks*" Thomas, F.; Debrie, F.; Gloanec, M.; Martin, P.; Ruggeri, S.; Uro, J.M. Custom Integrated Circuits Conference, 1988., Proceedings of the IEEE 1988 , 1988 Page(s): 9.1/1 -9.1/4

3 ED02AH GaAs IC Design Manuals

4 "*5 Gsample/s track-hold and 3 Gsample/s quasi-sample-hold ICs*" Lao, Z.; Thiede, A.; Lienhart, H.; Schlechtweg, M.; Bronner, W.; Hornung, J.; Hulsmann, A.; Jakobus, T. Solid-State Circuits Conference, 1998. Digest of Technical Papers. 1998 IEEE International , 1998 Page(s): 328 -329, 458

5 "*10 bit 200 MSPS GaAs BiFET sample and hold circuit*" Yu, J.; Beccue, S.; Ho, W.J.; Zampardi, P.; Chang, M.F.; Wang, K.C. Electronics Letters , Volume: 31 Issue: 16 , 3 Aug. 1995 Page(s): 1335 -1337

6 "*A 1 Gsample/s 8 b silicon bipolar track and hold IC*" Pregardier, B.; Langmann, U.; Hillery, W.J. solid-state Circuits Conference, 1995. Digest of Technical Papers. 41st ISSCC, 1995 IEEE International , 1995 Page(s): 58 -59, 340

7 "*25 Gb/s AGC amplifier, 22 GHz transimpedance amplifier and 27.7 GHz*" limiting amplifier ICs using AlGaAs/GaAs-HEMTs Zhihao Lao; Berroth, M.; Hurm, V.; Thiede, A.; Bosch, R.; Hofmann, P.; Hulsmann, A.; Moglestue, C.; Kohler, K.- Solid-State. Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International , 1997 Page(s): 356 -357, 485

8 CMP Circuits Multi Project Grenoble France

9 ALMA - Proposal for Phase 2: Construction - Volume 1. Executive summary (ESO, 22 Dec. 2000)

10 ALMA - Proposal for Phase 2: Construction - Volume 3. Technical Description (ESO, 22 Dec. 2000)

11 "Designing and Prototyping of 2-4 GHz Bandpass SiGe Digitizers and Associated Test Equipment for the ALMA project.I" Baudry A., Deschans D., Begueret J-B, Deval Y, Foullat P., Montignac G., Gentaz O., Torres M. ALMA memo no. 410 (2002)